Remarks/Arguments

The Examiner is thanked for the thorough examination and search of the subject.

Claims 43-74, 83, 84 and 89-102 are pending; Claims 43, 64 and 89 have been currently amended; Claims 1-42, 75-82 and 85-88 have been canceled. No new matter is believed to have been added.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicant respectfully traverses the rejections for at least the reasons set forth below.

Response to Claims 43-63

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As currently amended, independent Claim 43 is recited below:

43. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a first dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said first dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure, and said first contact point is at a

bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said metallization structure, and said second contact point is at a bottom of said second opening, wherein a gap is between said first and second contact points, wherein said passivation layer comprises an insulating nitride layer; and

a circuit trace over said passivation layer and on said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace is connected to said resistor through said first opening.

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Reconsiderations of Claims 43 and 48-53 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380), of Claims 54-59 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Erdejac et al. (U.S. Pat. No. 6,235,101), of Claims 60-63 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Sasagawa et al. (U.S. Pat. No. 6,486,530) or over Lin et al. in view of Woolery et al., Erdejac et al. and Sasagawa et al., of Claims 44-46 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Leidy (U.S. Pub. No. 2003/0155570), and of Claims 45 and 47 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Simila (U.S. Pub. No. 2003/0183332) are requested in accordance with the following remarks.

Applicant respectfully asserts that the chip structure currently claimed in Claim 43 patentably distinguishes over the citations by Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380).

The Examiner considers that "Lin discloses a chip structure comprising: ..... a resistor in said silicon substrate ..... a circuit trace

(26/22/36/28/38) over the passivation layer ..... wherein said circuit trace is connected to said resistor (col 4 lines 66-67, col 5 line 1-2 describe point of contact 16 as connected to the transistors and other devices on the surface of substrate 10, which would include the resistor. col 5 lines describe contact point 16 also in electrical contact with 22/36/38, which is the circuit trace. Thus the resistor on surface of substrate is connected to the circuit trace through contact 16) through said first opening (16)." and that "One of ordinary skill in the art at the time the invention was made would interpret "transistors and other devices" to include resistors, as transistor and resistors are known semiconductor devices that are commonly placed in substrates. This is further supported by many references, including the secondary reference Woolery which discloses a silicon substrate with transistors (440) and resistors (420) see Fig 4E. Additionally, other references disclosing metallization also disclose transistors and resistors within a substrate, for example U.S. Pat. No. 6,261,944 to Mehta et al. (col. 3, lines 45-57) and U.S. Pat. No. 5,328,553 to Poon (col. 5, lines 33-38)" *~ See lines 13 and 15 on page 2, lines 9 and 12-17 on page 3, and lines 3-10 on page 12, in the last Office Action mailed Jun. 1, 2009 ~*

Applicant respectfully traverses the Examiner's opinion. Lin's exact description does not include "a resistor in a silicon substrate", and thus the Examiner can not consider that Lin discloses the claimed subject matter of "a resistor in a silicon substrate".

As a matter of course, Lin fails to teach, hint or suggest that a circuit trace over a passivation layer can be connected to a resistor in a silicon substrate, because Lin's exact description does not include "a resistor in a silicon substrate".

Withdrawal of rejection under 35 U.S.C.103(a) to Claim 43 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent

Claim 43 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 44-63 patently define over the prior art as well.

Response to Claims 64-74, 83 and 84

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As currently amended, independent Claim 64 is recited below:

64. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said metallization structure, and said second contact point is at a bottom of said second opening, wherein a gap is between said first and second contact points, wherein said passivation layer comprises an insulating nitride layer; and

a circuit trace over said passivation layer and on said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace is connected to said resistor through said first opening, wherein said circuit trace comprises a titanium-containing layer and a gold layer over said titanium-containing layer.

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Reconsiderations of Claims 64, 69-74, 83 and 84 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380) and Sasagawa et al. (U.S. Pat. No. 6,486,530) or over Lin et al. in view of Woolery et al., Erdejac et al. (U.S. Pat. No. 6,235,101) and Sasagawa et al., of Claims 65-67 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Sasagawa et al., further in view of Leidy (U.S. Pub. No. 2003/0155570), and of Claims 66 and 68 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Sasagawa et al., further in view of Similа (U.S. Pub. No. 2003/0183332) are requested in accordance with the following remarks.

Applicant respectfully asserts that the chip structure currently claimed in Claim 64 patentably distinguishes over the citations by Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380) and Sasagawa et al. (U.S. Pat. No. 6,486,530).

The Examiner considers that "Lin discloses a chip structure comprising: ..... a resistor in said silicon substrate ..... a circuit trace (26/22/36/28/38) over the passivation layer ..... wherein said circuit trace is connected to said resistor (col 4 lines 66-67, col 5 line 1-2 describe point of contact 16 as connected to the transistors and other devices on the surface of substrate 10, which would include the resistor. col 5 lines describe contact point 16 also in electrical contact with 22/36/38, which is the circuit trace. Thus the resistor on surface of substrate is connected to the circuit trace through contact 16) through said first opening (16)." and that "One of ordinary skill in the art at the time the invention was made would interpret "transistors and other devices" to include resistors, as transistor and resistors are known semiconductor devices that are commonly placed in substrates. This is further supported by many references, including the secondary reference

Woolery which discloses a silicon substrate with transistors (440) and resistors (420) see Fig 4E. Additionally, other references disclosing metallization also disclose transistors and resistors within a substrate, for example U.S. Pat. No. 6,261,944 to Mehta et al. (col. 3, lines 45-57) and U.S. Pat. No. 5,328,553 to Poon (col. 5, lines 33-38)" *~ See lines 9 and 11 on page 7, lines 9 and 12-17 on page 8, and lines 3-10 on page 12, in the last Office Action mailed Jun. 1, 2009 ~*

Applicant respectfully traverses the Examiner's opinion. Lin's exact description does not include "a resistor in a silicon substrate", and thus the Examiner can not consider that Lin discloses the claimed subject matter of "a resistor in a silicon substrate".

As a matter of course, Lin fails to teach, hint or suggest that a circuit trace over a passivation layer can be connected to a resistor in a silicon substrate, because Lin's exact description does not include "a resistor in a silicon substrate".

Withdrawal of rejection under 35 U.S.C.103(a) to Claim 64 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent Claim 64 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 65-74, 83 and 84 patently define over the prior art as well.

Response to Claims 89-102

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As currently amended, independent Claim 89 is recited below:

89. A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said metallization structure, and said second contact point is at a bottom of said second opening, wherein a gap is between said first and second contact points, wherein said passivation layer comprises an insulating nitride layer; and

a circuit trace over said passivation layer and on said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace is connected to said resistor through said first opening, wherein said circuit trace comprises a copper layer.

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Reconsiderations of Claims 89 and 94-99 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380), of Claims 100-102 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al. and Sasagawa et al. (U.S. Pat. No. 6,486,530) or over Lin et al. in view of Woolery et al., Erdejac et al. (U.S. Pat. No. 6,235,101) and Sasagawa et al., of Claims 90-92 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Leidy (U.S. Pub. No. 2003/0155570), and of Claims 91 and 93 rejected under 35 U.S.C.

103(a) as being unpatentable over Lin et al. in view of Woolery et al., further in view of Simila (U.S. Pub. No. 2003/0183332) are requested in accordance with the following remarks.

Applicant respectfully asserts that the chip structure currently claimed in Claim 89 patentably distinguishes over the citations by Lin et al. (U.S. Pat. No. 6,495,442) in view of Woolery et al. (U.S. Pat. No. 6,528,380).

The Examiner considers that "Lin discloses a chip structure comprising: ..... a resistor in said silicon substrate ..... a circuit trace (26/22/36/28/38) over the passivation layer ..... wherein said circuit trace is connected to said resistor (col 4 lines 66-67, col 5 line 1-2 describe point of contact 16 as connected to the transistors and other devices on the surface of substrate 10, which would include the resistor. col 5 lines describe contact point 16 also in electrical contact with 22/36/38, which is the circuit trace. Thus the resistor on surface of substrate is connected to the circuit trace through contact 16) through said first opening (16)." and that "One of ordinary skill in the art at the time the invention was made would interpret "transistors and other devices" to include resistors, as transistor and resistors are known semiconductor devices that are commonly placed in substrates. This is further supported by many references, including the secondary reference Woolery which discloses a silicon substrate with transistors (440) and resistors (420) see Fig 4E. Additionally, other references disclosing metallization also disclose transistors and resistors within a substrate, for example U.S. Pat. No. 6,261,944 to Mehta et al. (col. 3, lines 45-57) and U.S. Pat. No. 5,328,553 to Poon (col. 5, lines 33-38)" *~ See lines 3 and 5 on page 4, lines 3 and 6-11 on page 5, and lines 3-10 on page 12, in the last Office Action mailed Jun. 1, 2009 ~*

Applicant respectfully traverses the Examiner's opinion. Lin's exact description does not include "a resistor in a silicon substrate", and thus the Examiner can not consider that Lin discloses the claimed subject matter of "a resistor in a silicon

substrate".

As a matter of course, Lin fails to teach, hint or suggest that a circuit trace over a passivation layer can be connected to a resistor in a silicon substrate, because Lin's exact description does not include "a resistor in a silicon substrate".

Withdrawal of rejection under 35 U.S.C.103(a) to Claim 89 is respectfully requested.

For at least the foregoing reasons, applicant respectfully submits independent Claim 89 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 90-102 patently define over the prior art as well.

Conclusion

Some or all Claims are believed to be in condition for Allowance, and that is so requested.

Sincerely yours,

/Winston Hsu/ Date: 08/24/2009

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)